ABSTRACT

Responding to a single command, a layout versus schematic (LVS) tool processes layout data describing positions of conductors on layers of an IC to produce data representing a shape recognition layer depicting boundary shapes of spirals of drawn inductors. The boundary shape of a spiral is the shape of the spiral as viewed from above with all of the layers of conductive material forming the spiral superimposed. The LVS tool then processes the shape recognition layer data to identify the type and position of each drawn inductor, to determine whether each inductor's spiral turns are of uniform width and spacing, to detect connectivity violations, and to determine parameters relating to the shape of the spiral from which its inductance can be computed.